Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(currently amended)   A method of interfacing for variable length packet and cell transfer between a first layer device and a second layer device comprising:

    (a)   dividing control information into an in-band portion and an out-of-band portion, said control information having a plurality of control words;

    (b)   transmitting the in-band portion of said control information along a path for data from one of said first and second layer devices to another of said first and second layer devices, wherein said in-band control information controls data bus lanes and not data;

    (c)   transmitting the out-of-band portion of said control information along a path for control/signaling from one of said first and second layer devices to another of said first and second layer devices; and

    (d)   inserting in said data path a control of data signal to identify when the data path contains control information and when it contains data;

whereby re-encoding of data and insertion of control information upon pre-

determined intervals is avoided.

2.(previously presented)   A method according to claim 1, wherein said in-band

portion is control information as to status and destination address of data being sent and

to align parallel data lines that comprise a data path and said out-of-band portion is

credit-based FIFO status flow control information;

whereby said interfacing is done independently in both transmit and receive directions

and a number of credits granted to each port depends on an encoded state of a

corresponding port status.

3.(original)   A method according to claim 2, including using a "1 1" framing pattern on

a FIFO status channel to mark boundaries of the framing pattern without requiring an out-

of-band framing signal.

4.(original)   A method according to claim 1, including sending a training control

pattern sufficiently often in order to allow a receive interface to check and correct for de-

skew on start-up and during regular operation to compensate for skew variations due to

changes in voltage, temperature, noise and other factors.

5.(original)   A method according to claim 1, using a clock in a direction opposite to the

data path as a reference source for the data path transmitting from a side of the interface

opposite to a transmitting end.

6.(currently amended)   A method according to claim 4, wherein a transmitting end

of the data path sends data and control signals precisely aligned with respect to a source-

synchronous clock and the training control pattern once every MAX_T where MAX_T is

configurable on start-up.

7.(currently amended)   A method according to claim 1, wherein said control

information has a plurality of control words and wherein each control word of said

control information contains an error-detection code and one or more control words are

inserted between bounded transfer periods whereby performance of the code is not

degraded by overly long transfers.

8.(original)   A method according to claim 1, wherein an end-of-packet event and error

codes are combined into a two-bit code to reduce the number of bits required.

9.(currently amended)   A method according to claim 1, wherein transfer

information referring to a previous transfer and to a next transfer is contained in one

control word of said control information.

10.(currently amended)   A method according to claim 1, wherein a single control

word of said plurality of control words may contain control information that applies to

data preceding said single control word as well as data following said single control

word.

11.(previously presented)   A method of interfacing for variable length packet and cell

transfer between a first layer device and a second layer device comprising:

(a)   dividing control information into an in-band portion and an out-of-

band portion;

(b) . transmitting the in-band portion of said control information along a

path for data from one of said first and second layer devices to

another of said first and second layer devices;

(c)   transmitting the out-of-band portion of said control information

along a path for control/signaling from one of said first and second

layer devices to another of said first and second layer devices;

(d)   inserting in said data path between data transfers a control of data

signal to identify when the data path contains control information

and when it contains data; and

(e)   transmitting FIFO status flow information out-of-band

whereby re-encoding of data and insertion of control information upon pre-

determined intervals is avoided.

12.(currently amended)   A method according to claim 11, wherein said first layer

device is a physical layer (PHY) and said second layer device has a transmit link layer

device operative to transmit data from said transmit link layer device to said PHY and a

receive link layer device operative to receive data from said PHY.

13.(currently amended)   A method according to claim 11, wherein said in-band

portion includes packet address, delineation and error control coding and said out-of-band

portion is FIFO status flow information whereby said an interface between said first layer

device and said second layer device operates independently in both transmit and receive

directions.

14.(currently amended)   A deskewing circuit for deskewing data arriving on a

plurality of data lines, comprising:

(a)   a plurality of serial-in parallel-out (SIPO) blocks, each of said

plurality of SIPO blocks coupled to a corresponding one of said plurality of data lines,

said SIPO blocks operative to convert n-bit words of serial input data from said plurality

of data lines to parallel data, where n is an integer;

(b)   M register[s] sets coupled to said plurality of SIPO blocks, each of

said register[s] sets operative to store a most recent W x n-bit words of data arriving on

each of said plurality of data lines, where M and W are an integer selected from the series

1, 2, ...K, where K is an integer;

(c)   a training detector block coupled to said M sets of registers and operative to detect the presence of a training pattern based on the contents of said registers;

(d)   a plurality of transition detection blocks each coupled to one of said M sets of registers and operative to search and to detect a transition in each bit position within each one of said M sets of W registers; and

(e)   an aligner block coupled to a plurality of said transition detection blocks operative to select appropriate bits within each of said M sets of registers from which to read each bit in order to present a deskewed output.

15.(currently amended)   A deskewing circuit, comprising:

(a)   17 serial-in parallel-out (SIPO) blocks, each one coupled to a corresponding input data line of a plurality of data lines which transmit serial data to said SIPO block and operative to convert serial input data to parallel output data, each of said SIPO blocks having n bit outputs where n is an integer equal to a word size of data output from each of said SIPO blocks, each of said SIPO blocks having separate bit outputs for each bit of an n-bit word contained therein;

(b)   ~~plurality of~~ M register~~[s]~~ sets coupled to said 17 SIPO blocks, each

of said M register sets operative to store most recent W x n-bit words of data arriving on

each of said plurality of input data lines, where W is the number of registers and M and

W are ~~integers~~ selected from the numbers in series 1,2, ...,K where K is an integer

(c)   a training detector block coupled to outputs of said ~~17~~ M sets of

registers operative to detect the presence of a training pattern based on the contents of

said M ~~17~~ sets of registers;

(d)   17 transition detection blocks coupled to respective outputs of said

M ~~17~~ sets of registers with each transition detection block having n*W inputs where n is

the number of bits in each register and W is the number of registers, when after the

presence of the ~~a~~ training pattern has been detected in one of said registers by an

associated one of said transition detection blocks, one of said transition detection blocks

is operative to search for a transition on one of said 17 bit positions; and

(e)   an aligner block coupled to outputs from said 17 transition

detection blocks operative to select an appropriate register and bit within said appropriate

register from which to read each bit in order to present a deskewed output.